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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,147	08/27/2003	Todd O. Bolken	03-0040.1	5050

22823 7590 03/24/2005

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EXAMINER

NOVACEK, CHRISTY L

ART UNIT PAPER NUMBER

2822

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary**Application No.**

10/649,147

Applicant(s)

BOLKEN ET AL.

Examiner

Christy L. Novacek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 51-95 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 57-76 and 81-95 is/are allowed.
- 6) ☒ Claim(s) 51-54, 56 and 77 is/are rejected.
- 7) ☒ Claim(s) 55, 78, 79 and 80 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the amendment filed December 20, 2004.

Response to Amendment

The amendment of claims 57 and 94 are sufficient to overcome the objections to claims 57 and 94 stated in the previous office action. Therefore, these objections are withdrawn.

The limitations added to claims 53, 57, 63 and 85 are sufficient to overcome the Nakayama et al. (US 6,621,172) reference. Therefore, the rejections of claims 53, 57, 59, 62, 63, 67, 70, 73, 85, 87, 90, 92 and 95 as being anticipated by Nakayama, the rejections of claims 60, 71, 88, 89, 91 and 93 as being unpatentable over Nakayama, the rejections of claims 64, 65, 86 and 94 as being unpatentable over Nakayama in view of Hayashida, and the rejection of claim 75 as being unpatentable over Nakayama in view of Chee are hereby withdrawn.

The limitations added to claims 51, 57, 63, 77 and 85 are sufficient to overcome the Jiang et al. (US 20030042615) reference. Therefore, the rejections of claims 51-53, 55, 63, 66 and 68 as being anticipated by Jiang, the rejections of claims 56-58, 61, 64, 65, 70, 72, 74, 77, 78, 80, 81, 83, 85-91 and 93-95 as being unpatentable over Jiang in view of Hayashida, the rejections of claims 60 and 71 as being unpatentable over Jiang, the rejections of claims 69 and 76 as being unpatentable over Jiang in view of Derderian, and the rejections of claims 79 and 84 as being unpatentable over Jiang in view of Hayashida and Derderian are hereby withdrawn.

Claim Objections

Claim 51 is objected to because of the following informalities: In line 16 of claim 51, “the second interconnects” should be changed to “the second interconnect contacts” (as recited in lines 4-5 of the claim). Appropriate correction is required.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 51, 52, 54 and 56 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakayama et al. (US 6,621,172).

Regarding claim 51, Nakayama discloses providing a substrate (70) having a plurality of first and second interconnect contacts (72), attaching a first die (50) to the substrate in electrical communication with the first interconnect contacts, forming a first encapsulant (74) on the first die such that at least one feature (74/76) on the surface of the encapsulant facilitates bonding to the first encapsulant, attaching a second die (60) to the surface of the first encapsulant and to the feature such that it is in electrical communication with the second interconnect contacts, and forming a second encapsulant (90) on the second die and on the first encapsulant (Fig. 1-3; col. 6, ln. 36 – col. 12, ln. 14).

Regarding claim 52, Nakayama discloses that the first encapsulant includes molding and the feature includes a molded feature.

Regarding claim 54, Nakayama discloses that the feature includes a molded ridge.

Regarding claim 56, a plurality of terminal contacts (80) is formed on the substrate in electrical connection with the first and second interconnect contacts (Fig. 1-3).

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Claims 51, 53, 56, and 77 are rejected under 35 U.S.C. 102(e) as being anticipated by Horiuchi et al. (US 6,731,010).

Regarding claim 51, Horiuchi discloses providing a substrate (23) having a plurality of first and second interconnect contacts, attaching a first die (25) to the substrate in electrical communication with the first interconnect contacts, forming a first encapsulant (37) on the first die such that at least one feature (52) on the surface of the encapsulant facilitates bonding to the first encapsulant, attaching a second die (55) to the surface of the first encapsulant and to the feature such that it is in electrical communication with the second interconnect contacts, and forming a second encapsulant (27) on the second die and on the first encapsulant (Fig. 4, 9A-9E; col. 10, ln. 30 – col. 11, ln. 67).

Regarding claim 53, Horiuchi discloses that the feature (52) is a layer of material applied to the surface (col. 10, ln. 57-63).

Regarding claim 56, Horiuchi discloses terminal contacts (22) on the substrate in electrical communication with the first and second interconnect contacts (Fig. 4).

Regarding claim 77, Horiuchi discloses providing a substrate (23) including a plurality of interconnect contacts and a plurality of terminal contacts (22) in electrical communication with the interconnect contacts, forming a plurality of die stacks on the substrate, each die stack comprising a first die (25) bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant (37) encapsulating the first die including a planar surface on the first die and a feature (52) on the planar surface configured to facilitate bonding to the first encapsulant and a second die (55) bonded to the first encapsulant in electrical

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communication with the interconnect contacts, and forming a second encapsulant (27) on the substrate encapsulating the die stacks (Fig. 4, 9A-9D; col. 10, ln. 30 – col. 11, ln. 67).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim 77 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. (US 6,621,172) in view of Hayashida et al. (US 6,767,767).

Regarding claim 77, Nakayama discloses providing a substrate (70) having a plurality of interconnect contacts (72) and a plurality of terminal contacts (80) in electrical communication with the interconnect contacts, forming a die stack on the substrate wherein each die stack includes a first die (50) in electrical communication with the interconnect contacts bonded to the substrate, a first encapsulant (74) having a planar surface and a feature (76) on the planar surface configured to facilitate bonding to the first encapsulant encapsulating the first die, and a second die (60) in electrical communication with the interconnect contacts bonded to the first encapsulant and forming a second encapsulant (90) on the substrate encapsulating the die stack. Nakayama shows only one portion of the substrate that is used to package one stack of semiconductor dice. Nakayama does not disclose how the entire substrate is laid out with die stacks. Hayashida discloses that the conventional way of packaging semiconductor die is attaching numerous die to a wiring board substrate, and packaging all of these die at the same time, thus efficiently forming multiple IC packages within the same process steps. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form multiple die stack packages on the substrate of Nakayama in an arrangement such as that taught by Hayashida

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because, for manufacturing efficiency purposes, it is well-known in the art to form multiple IC packages on the same wiring board substrate prior to singulation of individual packages.

Response to Arguments

Applicant's arguments filed December 20, 2004 have been fully considered.

Regarding the rejection of claim 51 as being anticipated by Nakayama, Applicant argues that Nakayama allegedly fails to teach forming a first encapsulant having a planar surface. However, this argument is moot with regards to claim 51, as claim 51 does not recite the limitation of forming a first encapsulant having a planar surface.

Allowable Subject Matter

Claims 55, 78, 79 and 80 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the indication of the allowable subject matter of claim 55 is the inclusion therein, in combination as currently claimed, of the limitation of forming a first encapsulant by molding with a mold cavity configured to form a feature on the surface of the encapsulant that facilitates bonding to the first encapsulant. This limitation is found in claim 55 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reason for the indication of the allowable subject matter of claim 78 is the inclusion therein, in combination as currently claimed, of the limitation of wire bonding the first die to the interconnect contacts. This limitation is found in claim 78 and is neither disclosed nor

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taught by the prior art of record, alone or in combination. Both Nakayama and Horiuchi teach flip-chip bonding the first die to the interconnect contacts.

The primary reason for the indication of the allowable subject matter of claim 79 is the inclusion therein, in combination as currently claimed, of the limitation of TAB bonding the first die and second die to the interconnect contacts. This limitation is found in claim 79 and is neither disclosed nor taught by the prior art of record, alone or in combination. Both Nakayama and Horiuchi teach flip-chip bonding the first die to the interconnect contacts and wire bonding the second die to the interconnect contacts.

The primary reason for the indication of the allowable subject matter of claim 80 is the inclusion therein, in combination as currently claimed, of the limitation of transfer molding the first encapsulant with a direct gate mold cavity configured not to contaminate selected interconnect contacts. This limitation is found in claim 80 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Claims 57-76 and 81-95 are allowed.

The primary reasons for the allowance of claims 57-62 is the inclusion therein, in combination as currently claimed, of the limitation of encapsulating the first die and the first interconnect contacts in a first encapsulant having a planar surface and a molded feature on the planar surface configured to facilitate bonding to the first encapsulant. This limitation is found in claims 57-62 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reasons for the allowance of claims 63-76 is the inclusion therein, in combination as currently claimed, of the limitation of providing a substrate on a leadframe, back

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bonding the first die to the substrate and encapsulating the first die and first interconnects in a first encapsulant having a planar surface. This limitation is found in claims 63-76 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reason for the allowance of claims 81-84 is the inclusion therein, in combination as currently claimed, of the limitation of back-bonding a first die to a substrate and encapsulating the first die such that the first encapsulant has a feature configured to facilitate bonding of the second die to the first encapsulant. This limitation is found in claims 81-84 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reasons for the allowance of claims 85-95 is the inclusion therein, in combination as currently claimed, of the limitation of encapsulating a first die with an encapsulant having a planar surface and a molded feature on the planar surface that facilitates bonding to the first encapsulant. This limitation is found in claims 85-95 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
March 17, 2005


AMIR ZARABIAN
SUPERVISOR-VENTE EXAMINER
COMMUNICATIONS SECTION